THE INVENTION CLAIMED IS:

1. A method for testing an integrated circuit (IC) comprising:

employing one of a plurality of input lines to receive a test signal for a processor;

employing one of a plurality of output lines to send a test result from the processor; and

if the test result is unsuccessful, performing at least one of:

employing a remaining one of the plurality of input lines to receive the test signal for the processor; and

employing a remaining one of the plurality of output lines to send the test result from the processor.

2. The method of claim 1 wherein employing one of the plurality of input lines to receive the test signal for the processor includes:

applying the test signal to each of the plurality of input lines;

selecting one of the plurality of input lines; and

receiving the test signal for the processor from the selected input line.

3. The method of claim 1 wherein employing one of the plurality of output lines to send the test result from the processor includes:

applying the test result to each of the plurality of output lines;

selecting one of the plurality of output lines; and

sending the test result from the processor using the selected output line.

4. The method of claim 1 wherein employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

selecting a remaining one of the plurality of input lines; and

employing the selected remaining one of the plurality of input lines to receive the test signal.

5. The method of claim 4 wherein selecting a remaining one of the plurality of input lines includes:

modifying a first select signal; and

selecting a remaining one of the plurality of input lines based on the modified first select signal.

6. The method of claim 1 wherein employing a remaining one of the plurality of output lines to send the test result from the processor includes:

selecting a remaining one of the plurality of output lines; and

employing the selected remaining one of the plurality of output lines to send the test result from the processor.

7. The method of claim 6 wherein selecting a remaining one of the plurality of output lines includes:

modifying a second select signal; and

selecting a remaining one of the plurality of output lines based on the modified second select signal.

8. The method of claim 1 wherein:

employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

selecting a remaining one of the plurality of input lines; and

employing the selected remaining one of the plurality of input lines to receive the test signal; and

employing a remaining one of the plurality of output lines to send the test result from the processor includes:

selecting a remaining one of the plurality of output lines; and

employing the selected remaining one of the plurality of output lines to send the test result from the processor.

9. The method of claim 8 wherein:

selecting a remaining one of the plurality of input lines includes:

modifying a first select signal; and

selecting a remaining one of the plurality of input lines based on the modified first select signal; and

selecting a remaining one of the plurality of output lines includes:

modifying a second select signal; and

selecting a remaining one of the plurality of output lines based on the modified second select signal.

10. An apparatus for testing an IC comprising:

a processor;

a plurality of input lines coupled to the processor;

a plurality of output lines coupled to the processor; and

a connector interface coupled to the plurality of input lines and the plurality of output lines;

wherein the apparatus is adapted to:

employ one of the plurality of input lines to receive a test signal for the processor;

employ one of the plurality of output lines to send a test result from the processor; and

if the test result is unsuccessful, perform at least one of:

employing a remaining one of the plurality of input lines to receive the test signal for the processor; and

employing a remaining one of the plurality of output lines to send the test result from the processor.

11. The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and

further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:

select one of the plurality of input lines; and

receive the test signal for the processor on the selected input line.

12. The apparatus of claim 11 wherein the first multiplexer is further adapted to:

select a remaining one of the plurality of input lines; and

employ the selected remaining one of the plurality of input lines to receive the test signal.

13. The apparatus of claim 11 further comprising a third multiplexer coupled to the connector interface and first multiplexer, and adapted to modify a first select signal, the first select signal corresponding to the first multiplexer; and

wherein the first multiplexer is further adapted to select a remaining one of the plurality of input lines based on the modified first select signal.

14. The apparatus of claim 10 wherein the processor is adapted to apply the test result to each of the plurality of output lines; and

further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, and adapted to:

select one of the plurality of output lines; and

send the test result from the processor using the selected output line.

15. The apparatus of claim 14 wherein the second multiplexer is further adapted to:

select a remaining one of the plurality of output lines; and

employ the selected remaining one of the plurality of output lines to send the test result from the processor.

16. The apparatus of claim 15 further comprising a third multiplexer coupled to the connector interface and second multiplexer, and adapted to modify a second select signal, the second select signal corresponding to the second multiplexer; and

wherein the second multiplexer is further adapted to select a remaining one of the plurality of output lines based on the modified second select signal.

17. The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and

further comprising a first multiplexer coupled to the plurality of input lines and the processor, the first multiplexer adapted to:

select one of the plurality of input lines; and

receive the test signal for the processor from the selected input line;

wherein the processor is further adapted to apply the test result to each of the plurality of output lines; and

further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, the second multiplexer adapted to:

select one of the plurality of output lines; and

send the test result from the processor using the selected output line.

18. The apparatus of claim 17 wherein:

the first multiplexer is further adapted to:

select a remaining one of the plurality of input lines; and

employ the selected remaining one of the plurality of input lines to receive the test signal; and

the second multiplexer is further adapted to:

select a remaining one of the plurality of output lines; and

employ the selected remaining one of the plurality of output lines to send the test result from the processor.

19. The apparatus of claim 18 further comprising a third multiplexer coupled to the connector interface, first multiplexer and second multiplexer, and adapted to:

modify a first select signal, the first select signal corresponding to the first multiplexer; and

modify a second select signal, the second select signal corresponding to the second multiplexer; and

wherein the first multiplexer is further adapted to select a remaining one of the plurality of input lines based on the modified first select signal; and

wherein the second multiplexer is further adapted to select a remaining one of the plurality of output lines based on the modified second select signal.

20. The apparatus of claim 10 wherein the connector interface is adapted to couple to a service processor.